REMARKS

Introduction

Applicant courteously submits these remarks in response to the non-final Office Action dated February 19, 2009 (hereafter referred to as "the Office Action" for convenience). Applicant respectfully asks for reconsideration of both this application and the Office Action.

A response to this Office Action was due by May 19, 2009. Accordingly, Applicant is submitting a Petition for a three month extension of time with this Amendment. The Commissioner is authorized to charge the associated Petition fee of $1,110, together with any other fees that may be necessary for the entry and consideration of this Amendment and to maintain the pendency of this application, including any fees under 37 C.F.R. §1.16 or §1.17, to Deposit Account No. 50-4256. The period for responding to the outstanding Office Action is thus extended up to and through the 19th of August 2009. Please consider this Amendment as timely filed.

Applicant respectfully points out that claims 8, 9, 10, and 32 have been canceled without prejudice or disclaimer. Further, claims 1, 2, 16, 17, 19, 20, 23, 26 and 29-31 are amended to better recite various features of the invention. Applicant courteously urges that no new matter is presented by these amendments.

Applicant gratefully acknowledges the telephonic interview granted by the Examiner on July 22, 2009. During that interview, Applicant discussed distinctions between various embodiments of the invention and the system disclosed in the U.S. Patent Publication No. 2002/0065642 to Swoboda. In particular, it was noted that various implementations of the

invention compacts the state data by sorting the data of interest from the ignored data, whereas the Swoboda publication discloses the use of a compression scheme to compact data. Further, Applicant explained that both the use of the terms "state data" and "data of interest" as recited in the claims. This Amendment is presented in accordance with the substance of that interview.

Rejections Under 35 U.S.C. § 112 ¶ 2

Claims 1, 2, and 16 – 19 are rejected under 35 U.S.C. § 112 ¶ 2 as failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully traverses this rejection.

The Office Action asserts at page 5 that "neither claim nor specification defines 'state data' and how a subset of that is selected to arrive at 'data of interest'." Applicant contends that one of ordinary skill in the art is capable of discerning the meaning of "state data," "data of interest," and how such is selected as the terms have been used by those of skill in the art to refer to data representing specific states of elements or components of a device or design and portions of the state data that are interesting to the designer, developer or user respectively. The Manual of Patent Examining Procedure (MPEP) § 2173.02 states:

> The requirement to 'distinctly' claim means that the claim must have a meaning discernible to one of ordinary skill in the art when construed according to correct principles. (*Metabolite Labs., Inc. v. Lab. Corp. of Am. Holdings*, 370 F.3d 1354, 1366, 1089 Fed. Cir. 2004). Accordingly, a claim term that is not used or defined in the specification is not indefinite if the meaning of the claim term is discernible [to one of ordinary skill in the art].

Although Applicant maintains that "state data" and "data of interest" are sufficiently definite, Claim 1 has been amended to define state data as "being descriptive of one or more states in an

emulation system." This definition is consistent with the definition commonly used in the art to refer to state data as well as the manner used in the specification (e.g. see ¶ 31 of the specification, "the first select logic device **310** successively receives samples of state data read out from various state elements of the emulation design emulated by the reconfigurable resources included in the emulation IC **120**").

Furthermore, Claim 1 has been amended to recite "identifying a first data of interest in the first sample of state data, wherein the first data of interest is a subset of the first sample of state data." The specification states at ¶ 31 that "the first select logic device **310** (under the control of a control station in one embodiment) directs each of the successively received samples of state data to either the first buffer **320** or the second buffer **325**… Successively received samples of state data may be sorted, indexed to memory, and/or compacted into successive samples of sorted data, comprising data of interest." Accordingly, the data of interest is selected, or identified from the state data "under the control of a control station". The specification in ¶ 36 states that "[d]ata of interest sorter **440** may be software driven, hardware driven, or a combination of software and hardware driven." Accordingly, specific portions of state data that are "of interest" and as a result comprise the "data of interest" may be determined by either hardware, software, or both. Additionally, a user of the invention may operate the control station such that the portions of the state data that are of interest to the user are selected.

In view of the above amendment and remarks, Applicants submit that claims 1, 2, 8, 16 – 19 are definite and that the rejection under 35 U.S.C. § 112 ¶ 2 be withdrawn.

Rejections Under 35 U.S.C. § 103

Claims 1, 2, and 16 – 31 are rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent Publication No. 2002/0065642 (Swoboda) in view of U.S. Patent No. 6,816,989 (Litt) and further in view of U.S. Patent No. 6,092,127 (Tausheck).

Regarding Independent Claim 1

Claim 1 now recites "sorting the first data of interest from the first ignored data by storing the first data of interest in the first buffer" [or the second buffer if it is determined that residual storage space in the first buffer does no exist]. Swoboda, Litt, and Tausheck, both individually and in combination fail to teach or suggest this feature of the invention. Particularly, Swoboda teaches a method of lossless compression. "In FIG. 19 [data compression map], the shaded bytes correspond to the 0's in the data compression map, and only these bytes will be sent. The trace packet decoder in FIG. 2 can easily decode the data compression map and determine therefrom which bytes are being transmitted and which bytes are merely duplicated and therefore not transmitted." The data compression map of Swoboda is generated and transmitted by the emulation system in addition to those portions of the state data corresponding to 0's in the data compression map. As a result, the entire state data may be recreated and displayed by the trace display of FIG. 2.

Although the method of Swoboda deals with transmission of state data, the method requires the generation and subsequent transmission of a compression map. Swoboda does not work without the compression map (i.e. Fig. 19). As stated, Swoboda is a method of lossless

compression. Particularly, Swoboda transmits all state data that is not duplicative, along with a data compression map highlighting which portions of the state data were duplicative and which were not. Claim 1 is directed towards a method of lossless compression. Particularly, Claim 1 transmits only those portions of the state data that are of interest to the user. More particularly, the user selects through a control station those portions of the state data that are of interest. Only the portions of the state data designated by the user are transmitted. Claim 1 does not have anything equivalent to the data compression map of Swoboda. Removal of the data compression map from Swoboda renders Swoboda unsatisfactory for its intended purpose of compressing state data for transmission while preserving the entire state data. Swoboda is different from and does not render obvious Claim 1 for at least the above highlighted reason.

Additionally, as Swoboda does not work without the data compression map, there is no suggestion or motivation to combine any elements from Claim 1 anticipated by Swoboda with either Litt or Tauscheck (see MPEP § 2143.01(V) and (VI)). Moreover, Litt and Tausheck fail to remedy the deficiencies of Swoboda. Litt merely discusses bandwidth manager 125 that selects data from two or more data streams within an integrated circuit, where the incoming data sources represent state data from regions within the integrated circuit. The selection of the incoming data stream is determined by signal VP (as shown in Fig. 2 but not numbered), which may be based on a configuration and status register. (Column 8, lines 34-48.) Tausheck merely discusses allocating a second buffer when a first buffer if filled when accessing a FIFO memory. (Column 2, lines 20-45.)

In view of the above amendments and remarks, Applicant respectfully submits that Claim 1, and as a result, dependants Claims 2, and 16 – 19 are patentable over Swoboda in view of Litt and further in view of Tausheck.

Regarding Independent Claims 29, 30, and 31

Applicant is amending the claim to include the feature of "determining a schedule for associating a plurality of pins with the plurality of trace data chains to transfer data out of the trace data chains based at least upon the determined trace data chain fill rates, wherein one of the plurality of pins is shared by at least two trace data chains and wherein the plurality of pins changes from a first clock cycle to a second clock cycle." The amendment is supported by the specification as originally filed, e.g., ¶ 58. Applicant is similarly amending independent claim 30 to include the feature of "associating a set of the plurality of trace data chains with the plurality of pins in accordance with the determined schedule, wherein one of the plurality of pins is shared by at least two trace data chains and wherein the plurality of pins changes from a first clock cycle to a second clock cycle." Applicant is also amending independent claim 31 to include the feature of "a memory coupled to the trace pin select logic device and configured to store a schedule to associate the selected set with the pins based at least upon determined trace data chain fill rates of the set, wherein one of the plurality of pins is shared by at least two trace data chains and wherein the plurality of pins changes from a first clock cycle to a second clock cycle."

Regarding independent claim 29, Swoboda, Litt, and Tausheck, either individually or in

combination, fail to suggest the feature of "determining a schedule for associating a plurality of pins with the plurality of trace data chains to transfer data out of the trace data chains based at least upon the determined trace data chain fill rates, wherein one of the plurality of pins is shared by at least two trace data **chains and wherein the plurality of pins changes from a first clock cycle to a second clock cycle**." (Emphasis added.) The Office Action admits at page 14 that Litt does not teach a pin manager explicitly that would perform the steps of offloading the data. Furthermore, the Office Action asserts at page 14 that Swoboda teaches pin manager and pin macros for identification of output pins where the trace will be outputted, chains as plurality of pins in the trace output where there are a plurality of trace data chains.

Swoboda merely discusses determining the debug pin utilization at the beginning of a debug session (see ¶ 73) and appears to restrict the debug pin configuration to a static configuration during the debug session. While Swoboda discusses a sharing of pins option, Swoboda fails to suggest changing the shared pins from one clock cycle to another. Moreover, Tausheck fails to remedy the deficiencies of Litt and Swoboda.

Similarly, claim 30 includes the feature of "associating a set of the plurality of trace data chains with the plurality of pins in accordance with the determined schedule, wherein one of the plurality of pins is shared by at least two trace data chains and wherein the plurality of pins changes from a first clock cycle to a second clock cycle," and claim 31 includes the feature of "a memory coupled to the trace pin select logic device and configured to store a schedule to associate the selected set with the pins based at least upon determined trace data chain fill rates

of the set, wherein one of the plurality of pins is shared by at least two trace data chains and wherein the plurality of pins changes from a first clock cycle to a second clock cycle."

Consequently, claims 30 and 31 are patentable for at least the above reasons.

Conclusion

In view of the above amendments and remarks, Applicants respectfully submit that all of the currently pending claims are now patentable and that this application is therefore in a condition for allowance. Favorable action in this regard is courteously requested at the Examiner's earliest convenience.

Respectfully submitted,

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